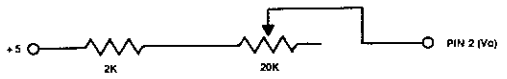
VIEWING DIRECTION ADJUSTMENT

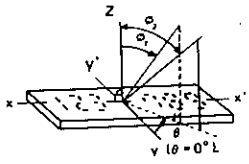
The viewing angle for the Series 3802 Displays is a constant arc which is nominally ±20° to the angle of maximum contrast ratio. The viewing angle control adjusts this angle at maximum contrast with respect to the display front surface to provide optimum reading ability from any viewing level. To allow an adjustable viewing direction connect a 20K Ohm potentiometer in series with a 2K resistor from +5 volts to Pin 2 (Vo) of the module (see diagram). For viewing from a fixed angle, a resistor with a value of between 2K Ohms and 20K Ohms may be selected.



OPTICAL DATA

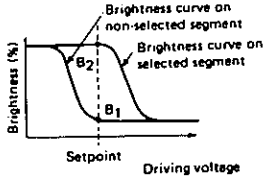
Item	Mark	Condition	Min.	Normal	Max.	Remarks
View angle	ϕ_2-ϕ_1	θ=0°,K=1.4	20°	–	–	See Note 1,2
Contrast	K	ϕ_2-ϕ_1=25°,θ=0°	–	3	–	See Note 1,2
Optical response Rise time	tr	Ta=25°C ϕ_2-ϕ_1=25°,θ=0°	–	200 ms	400 ms	See Note 1,3
Optical response Decay time	tf	Ta=25°C ϕ_2-ϕ_1=25°,θ=0°	–	200 ms	400 ms	See Note 1,3

Note 1. Definition of angle θ and ϕ

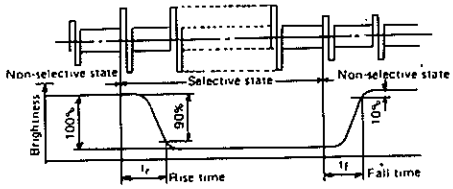


Note 2. Definition of contrast "K"

$$K = \frac{\text{Brightness on non-selected segment } (B_2)}{\text{Brightness on selected segment } (B_1)}$$



Note 3. Definition of optical response



ELECTRICAL CHARACTERISTICS (Vss = OV, Vdd 5V ± 5% Ta = 0°C — 50°C)

ITEM		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Voltage		V_{IH}	2.0			V	1
TTL Compatible		V_{IL}			+0.8	V	1
Output Voltage	0.205mA	V_{OH}	+2.4			V	DB7
	1.6mA	V_{OL}			V_{dd} + 0.4	V	DB7
Input Leakage Current		$\pm I_{IN}$			5	μA	1
Output Leakage Current		$\pm I_{LO}$			10	μA	DB7
Input Pull Up Current		I_{PL}	2	10	20	μA	1
Power Dissipation		P_d			10	mW	

NOTES:

1) E, R/W, A0, DB0-7

ENVIRONMENTAL CHARACTERISTICS

Storage Temperature..... −20°C to 602°C
Operating Temperature.....0°C to 50°C
Humidity (40°C)..... 95% RH (non-condensing)
Humidity (40°C)..... absolute humidity must be lower than the humidity of 95% RH at 40°C
Vibration.....0.5g
Shock (operating).....3g
Shock (storage).....5g

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V_{dd})..... −0.3 ~ +7.0V
Input Voltage (V_t)..... −0.3V ~ +V_{dd} +0.3V

POWER CONSIDERATIONS

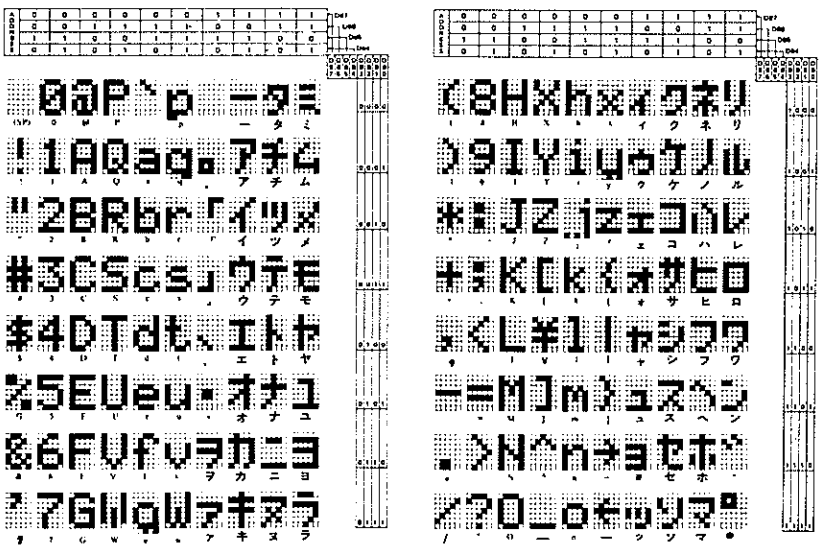
Power supplies (V_{DD} —.V_{SS})..... +5 ± 0.25V
Current consumption +5V..... 1mA max.
Input high voltage.....0.7 V_{DD} min.
Input low voltage.....0.3 V_{DD} max.

PIN DESCRIPTIONS

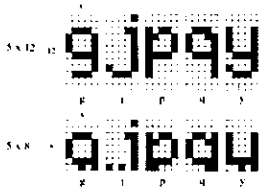
PIN NO.	SYMBOL	FUNCTION
1	V_{SS}	Power supply - ground
16	V_{DD}	Power Supply 5VDC ± 0.25V
2	V_O	Viewing angle adjustment voltage
15	A0	Register select. Set high to input alphanumeric data. Set low to input control data.
3	R/W	READ/WRITE select. Hold low to write alphanumeric or control data to display. Hold high to read Busy Flag (Data Bit 7).
14	E	Enable pulse. Data is clocked into the DAYSTAR Module on the trailing edge of this pulse. Valid Busy Flag data appears on Data Bit 7, a maximum of 300 nS after the leading edge of this pulse and is valid for 10 nS after the trailing edge.
4 13 5 12 6 11 7 10	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	8 bit data bus over which alphanumeric and control data is sent. Data bit 7 is bi-directional so that Busy Flag status can be read over it.
8,9	CS1,CS2	Chip select 1, chip select 2. These are active high chip selects. When the device is not selected, the 8 bit bus is tri-stated (floated). The device must be selected to write to it or read from it. When not used, CS1 and CS2 should be tied high.

PIN NUMBER	FUNCTION
1	Power Ground
2	V_O Viewing Angle
3	R/W
4	Data Bit 0
5	Data Bit 2
6	Data Bit 4
7	Data Bit 6
8	Chip Select 1
9	Chip Select 2
10	Data Bit 7
11	Data Bit 5
12	Data Bit 3
13	Data Bit 1
14	Enable
15	A0
16	Power +5VDC

FONT TABLE

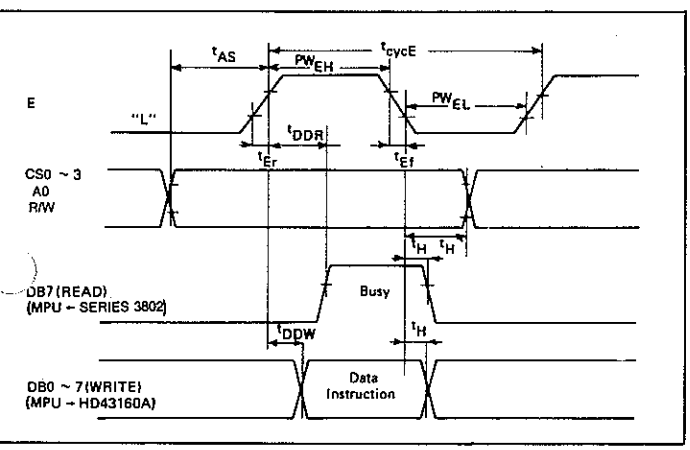


LOWER CASE CHARACTERS



CURSOR OPTIONS

TIMING DIAGRAM



Item	Symbol	Test Condition	Min.	Typ.	Max.	Units	Terminal Name
Enable Cycle Time	t_{cycE}	Switching Waveform 1	1000			nS	E
Enable Pulse Width (High Level)	PW_{EH}	Switching Waveform 1	450			nS	E
Enable Pulse Width (Low Level)	PW_{EL}	Switching Waveform 1	450			nS	E
Enable Rise/Fall Time	t_{Er}, t_{Ef}	Switching Waveform 1			25	nS	E
Setup Time	t_{AS}	Switching Waveform 1	140			nS	CS0,1; A0; R/W
Hold Time	t_H	Switching Waveform 1	10			nS	CS0,1; A0; R/W; DB0 7
Data Delay Time (Write)	tDDW	Switching Waveform 1	225			nS	DB0 ~ 7
Data Delay Time (Read)	t_{DDR}	Switching Waveform 1			300	nS	DB7